CISC

RISC

Variable length instructions

Fixed length instructions

Instructions require multiple clock cycle to execute

(Includes multi-clock complex instructions )

One cycle execution, (Includes single-clock reduced

instructions only), supports pipelining:

simultaneous execution of parts, or stages of

instructions

Memory-to-Memory: LOAD and STORE are

incorporated in the instruction

Register-to-Register: LOAD and STORE are

independent instructions

More complex addressing modes

As simple as possible

Small number of general purpose registers, Several

special purpose registers

Large number of registers organised into a register

file (prevent large amount of interaction with the

memory), Limited or no special function registers

Emphasis on hardware: Fewer instructions to

complete a given task, Less complex compiler

(Small code sizes, high cycles per second)

Emphasis on software: More instructions to

complete a given task, complex compiler (Low

cycles per second, large code sizes)

Micro-coded control unit

Hardwired control unit

Transistors used for storing complex instructions

Spends more transistors on memory registers